

# Oxide materials for III–V MOSFET gate stacks

**After a 40 year search, there is new incentive and opportunity to find suitable 'gate oxides' for III–V semiconductors. Success could lead to early adoption of III–V materials and capabilities into mainstream logic device production, reports Dr Mike Cooke.**

**T**he overwhelming majority of existing electronics devices — for example, computers and peripherals, home and mobile entertainment, and communication systems etc — are based on billions of metal–oxide–semiconductor field-effect transistors (MOSFETs) fabricated in silicon. Over the years, these silicon MOSFETs have provided lower power consumption, higher operating frequency and higher complexity at low cost.

III–V semiconductor materials are only used for the electronic functions that cannot be implemented effectively in silicon. The most important of these is the production of light, where compound semiconductor materials are needed to provide high-efficiency photon-producing transitions in diode structures.

Another important use of compound semiconductors is for high-speed transistor devices, such as in power amplifiers for radio frequency communications (e.g. mobile phone handsets and network base-stations). These transistors take advantage of the higher mobility and higher saturation velocities (peak carrier velocity at high field) of compound semiconductor materials.

Although high-speed III–V devices often consist of field-effect transistors of some sort, these are quite different from MOSFETs in not usually having a gate insulator layer, but rather they use the Schottky barrier of a direct metal-semiconductor contact (MESFETs). Heterostructure layers are also used to create two-dimensional electron gases in quantum wells away from the gate in high-electron-mobility transistors (HEMTs), also known as modulation-doped FETs (MODFETs).

While devices with a high cut-off frequency can be fabricated, there are often limitations in terms of gate leakage currents, and it is difficult to produce

normally-off (enhancement-mode) components rather than normally-on (depletion-mode) components. Gate-leakage and normally-on currents both waste power. These features hamper the use of compound semiconductors with efficient power handling.

This means that high-frequency devices have had to be specially designed to operate within the constraints of these compound semiconductor devices. Attempts over some 40 years to find gate insulators for compound semiconductors that can do a similar job to that carried out by silicon dioxide in CMOS have proved largely fruitless.

Meanwhile, in the silicon semiconductor sphere of influence, CMOS development has been steadily increasing its operating frequency, lowering power requirements and creating ever smaller devices. This has been the result of the ability, until relatively recently, to scale CMOS — the use of essentially the same device structure at a smaller scale allows higher cut-off frequencies and lower supply voltages.

## New challenges/opportunities

However, as CMOS technology passed from the tenths of micron to tens of nanometer scale at the turn of the millennium, there have been some important changes due to 'short-channel effects', i.e. effects that are ignorable at larger scales make their presence increasingly felt as devices continue to shrink.

One of the leading MOSFET research projects of recent years has been to change the gate insulator from silicon dioxide to a thicker, higher-k dielectric constant material; this is because continuing with SiO<sub>2</sub> would have required insulation consisting of just a few atomic layers, leading to reliability problems. A stop-gap solution was to patch-up SiO<sub>2</sub> with nitrogen (SiON) to allow the 'equivalent oxide thickness' (EOT) to scale down while the physical thickness remains large enough for reliability requirements.

In the next few years, the industry is expected to transfer the gate dielectric to even higher-k materials such as HfSiON or HfO<sub>2</sub>. This will also require the use of metal rather than the traditional polysilicon electrodes.

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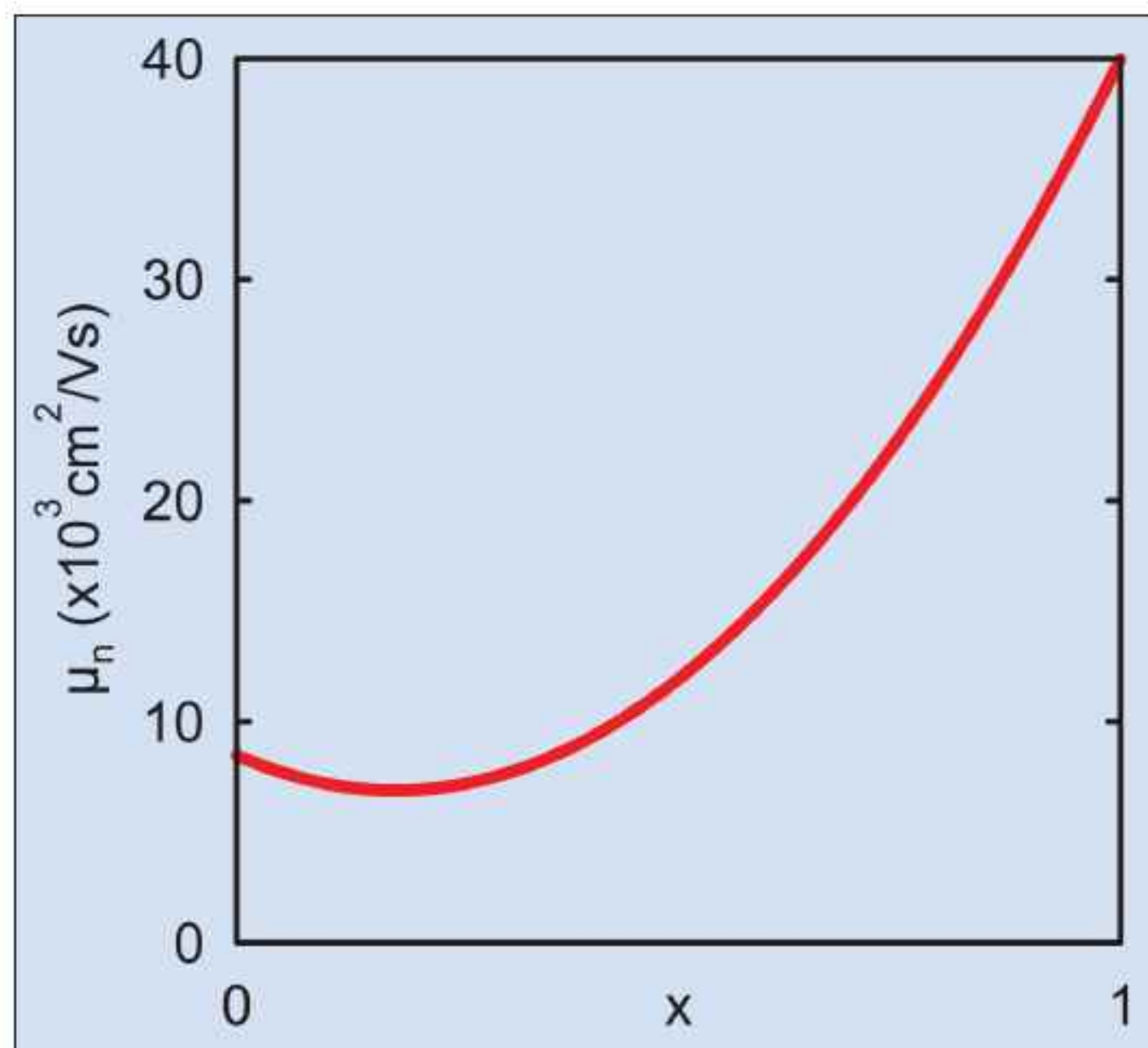
The metal that is used needs to be carefully matched to the properties of the high-k dielectric and the channel.

Another important need is to increase the channel mobility. One reason for this is that the traditional scaling equation requires ever increasing doping levels. The doping levels now needed to continue MOSFET development adversely affect the channel resistance away from the scaling assumptions, hitting the power efficiency and performance. Increasing the channel mobility would shift the resulting MOSFETs into more comfortable doping levels. Delta-doping — doping outside the channel, as used in many III-V devices — could even lead to use of undoped channels.

Introducing strain (i.e. stretching or compressing the channel) has already been used by the silicon CMOS industry to achieve some level of mobility enhancement, but this is a limited solution. Work has already started on changing the channel material. For the PMOSFET side of the complementary MOSFET (CMOS) system, germanium channels seem a promising way forward. The hole mobility of germanium is  $1.8 \times 10^3 \text{ cm}^2/\text{Vs}$ , compared with silicon's  $0.5 \times 10^3 \text{ cm}^2/\text{Vs}$ . However, for NMOSFETs some III-V material is favored. For example, Intel has worked with Qinetiq and IQE on developing transistors based on InSb and InGaAs, respectively. In either case, hetero-integration of the III-V channel with silicon substrates — which is needed to enable low-cost production on large substrates — has been demonstrated over the past few years. It is the 'gate oxide' insulation that is presently lacking.

In many ways, the search for suitable high-k dielectric materials for silicon channels has reopened the question of finding gate insulators for other channel materials. In addition, the precision techniques used or proposed for depositing high-k materials on silicon owe much to those developed for compound semiconductors, such as metal-organic chemical vapor deposition (MOCVD). Furthermore, newly applied techniques such as atomic layer deposition (ALD) could allow further variations.

In the past few years, a number of university groups have been exploring new possibilities for 'gate oxides' on III-V channel layers, much of this in the InGaAs system with a view to digital CMOS application beyond the '22nm node'. The International Technology Roadmap for Semiconductors (ITRS) estimated in its 2007 edition that this node will be with us around 2016 [1]. At the moment, the ITRS sees III-V implementation only coming later than this, after double-gate and even triple-gate structures (aimed at providing improved control of channel currents). However, these architectures require sophisticated three-dimensional structuring that may be difficult to achieve reliably. A high-mobility III-V channel solution could be used to maintain the simpler traditional planar structure for longer.



**Figure 1. The electron mobility of In<sub>x</sub>Ga<sub>1-x</sub>As at 300K, as given by the following formula:**

**$\mu = (8.5 - 17.7x + 49.2x^2) \times 10^3 \text{ cm}^2/\text{Vs}$  [2]. The top mobility of  $40 \times 10^3 \text{ cm}^2/\text{Vs}$  for pure InAs compares with InSb's  $77 \times 10^3 \text{ cm}^2/\text{Vs}$ . The mobility of silicon is a mere  $1.5 \times 10^3 \text{ cm}^2/\text{Vs}$ .**

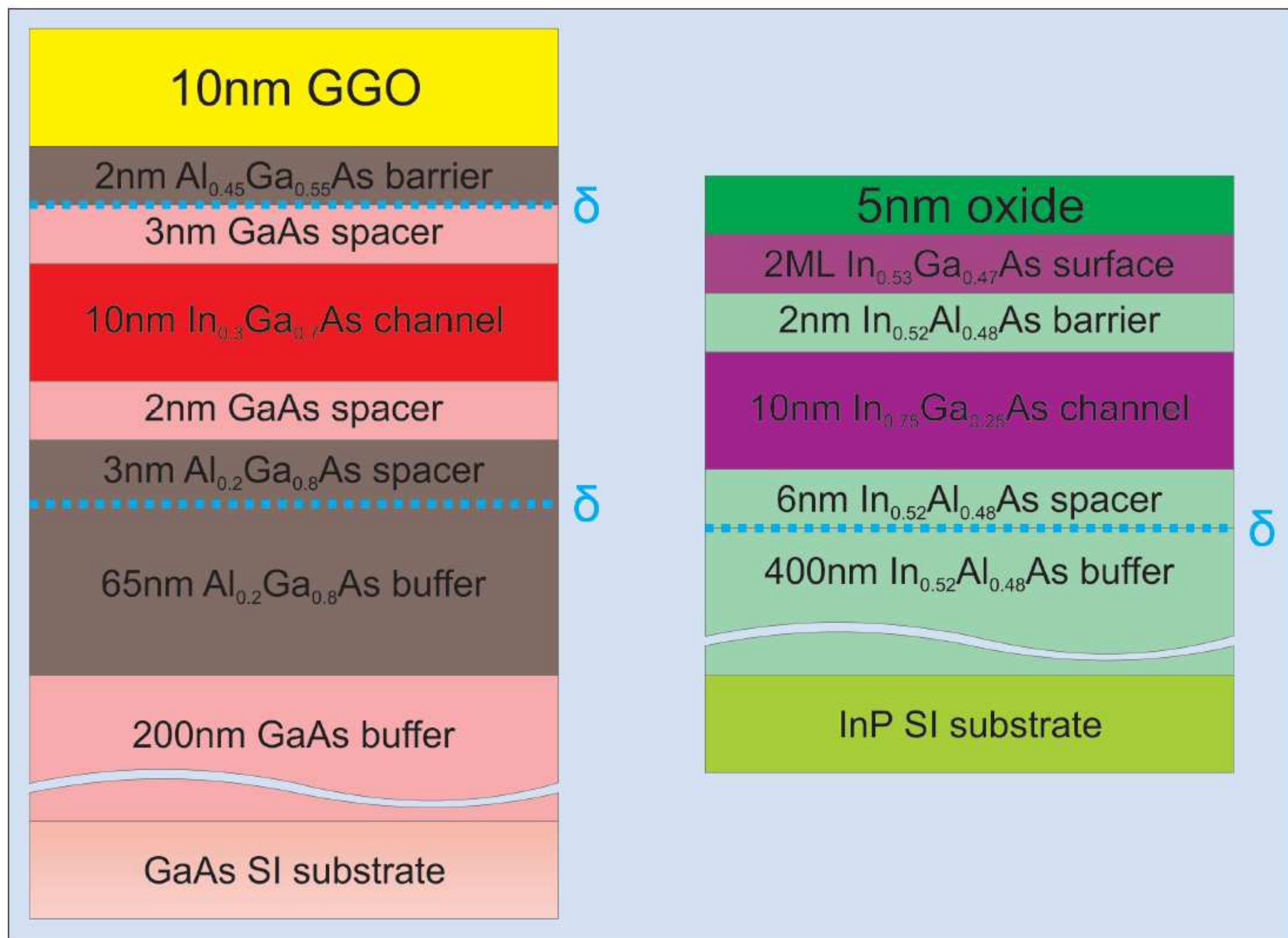
### Avoiding traps

One of the leading problems for gate insulator layers is that charge trap states can develop near interfaces with other materials. If charge is trapped in the interface region, this shifts the potential in the channel, affecting the all-important threshold voltage for the switch-on of currents in the transistor. The SiO<sub>2</sub>/Si combination has been particularly good at avoiding such trap states.

One group looking for 'gate oxide' solutions for high-mobility channels is based at University of Glasgow under the direction of professor Iain Thayne. The research at Glasgow is aimed at finding III-V digital solutions for implementation beyond the 22nm node.

Although the team has validated GaAs MOSFETs with Freescale Semiconductor, this channel material will never achieve the necessary drive current in the channel and access resistances required. These features are needed to create devices that operate at low power with a low supply voltage. For GaAs, the Glasgow-Freescale research showed that Ga<sub>2</sub>O<sub>3</sub> was a suitable insulator with low enough concentrations of trap levels.

Introducing indium to produce In<sub>x</sub>Ga<sub>1-x</sub>As can boost mobility (Figure 1), thereby increasing conductivity and drive currents. High-indium-concentration InGaAs, or perhaps even InAs, would give devices that could be used to continue semiconductor development both in terms of higher-frequency and low-power-loss performance. For InGaAs, the challenge is now to produce an



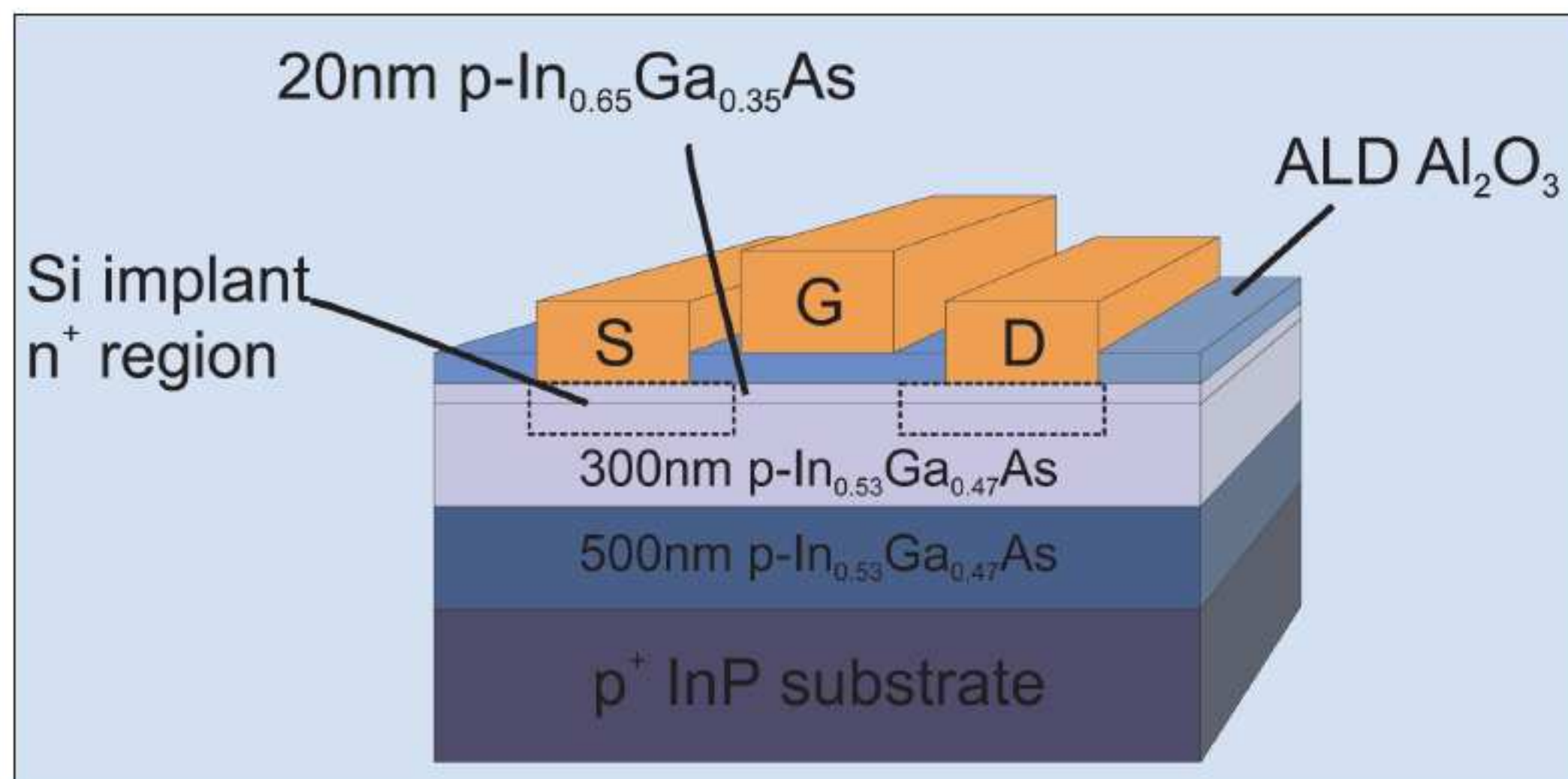
**Figure 2.** The layer structures of (left) an  $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$  channel device on a GaAs substrate [3] and of (right) an  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$  channel device on an InP substrate [4], as developed by Glasgow and Freescale.

insulator with a high  $k$  dielectric constant with low trap densities ( $<10^{11}\text{cm}^{-2}$ ).

More recent Glasgow research has been on InGaAs channels with increasing fractions of indium, much of this is on  $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$  on GaAs substrates [3], although some

work on  $\text{In}_{0.75}\text{Ga}_{0.25}\text{As}$  on InP has been carried out recently [4]. As can be seen in Figure 1, the  $x = 0.3$  InGaAs gives no improvement in mobility over pure GaAs.

Both of these devices use III-V AlGaAs barriers and silicon delta-doping just outside the channel (Figure 2).



**Figure 3.** Schematic of Purdue University's  $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}$  channel device [5].

The GaAs-substrate transistor has a gate length of 180nm, while the InP device is for these days a massive  $1\mu\text{m}$  (1000nm).

Increased indium concentration increases the currents achieved in the on-state, but difficulties in turning off the device are attributed to trap states in the high- $k$  metal oxide ( $k=20$ ) layer. This high-indium-concentration device achieved typical maximum drive currents ( $I_{d,\text{sat}}$ ) of  $933\mu\text{A}/\mu\text{m}$ , extrinsic transconductances ( $g_m$ ) of  $737\mu\text{S}/\mu\text{m}$ , gate leakages

( $I_g$ ) of 40pA, and on-resistances ( $R_{on}$ ) of 555 $\Omega$ m. The metal oxide is not specified. For the lower-indium-concentration device, an  $Ga_2O_3/(Ga_xGd_{1-x})_2O_3$  (GGO) stack grown by molecular beam epitaxy (MBE) was used. Such a stack can have  $k$  values of about 20, compared with  $SiO_2$ 's 3.9. The figures of merit for the low-indium device were an  $I_{d,sat}$  of 386 $\mu$ A/ $\mu$ m ( $V_g = V_d = 1.5$ V),  $g_m$  of 426 $\mu$ S/ $\mu$ m,  $I_g$  of 44nA/ $cm^2$ , and  $R_{on}$  of 1640 $\Omega$ m.

Another group researching InGaAs MOSFETs is led by Peide Ye at the USA's Purdue University. The Purdue group uses atomic layer deposition of  $Al_2O_3$  and other materials to create gate oxides. An  $In_{0.65}Ga_{0.35}As$ -channel device (Figure 3) has achieved a gate leakage of less than  $5 \times 10^{-6}$ A/ $cm^2$  with a 4V gate bias [5]. The gate length of the device was 0.4 $\mu$ m. The maximum drain current (1.05A/mm) and transconductance (350mS/mm at a drain voltage of 2V) are claimed to be record high values for III-V MOSFETs.

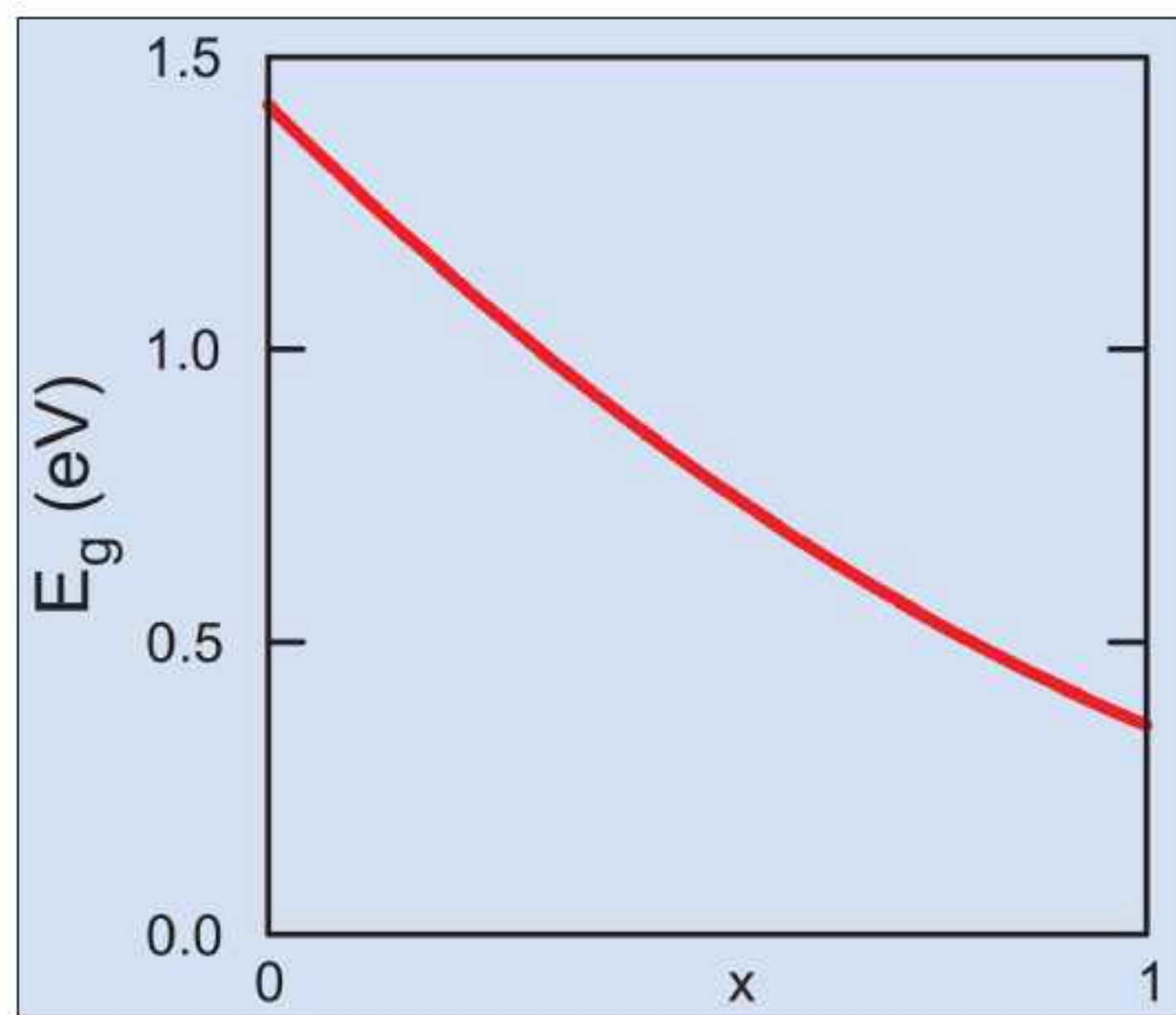
Purdue has also carried out preliminary work in collaboration with Lightspin Technologies and Yale University on ALD of  $Al_2O_3$  on even higher-mobility InAs, building MOS test structures and FETs without source/drain implants [6]. Single-crystal InAs substrate wafers were used. One InAs MOS structure showed a gate leakage of less than  $10^{-8}$ A/ $cm^2$  at biases lower than 10V, and some capacitance-voltage (CV) measurements were carried out. The FETs had a transconductance of about 2mS/mm.

The other material touted as a possible high-mobility channel material is InSb, for example by Qinetiq and Intel. The mobility of InSb is about 77,000 $cm^2/Vs$ . The devices produced up to now have effectively been HEMT-type structures that consequently suffer from gate leakage currents that are too high. Again, the challenge is to produce suitable insulation of the gate electrode. Much of the work here seems to be in the simulation stage (with  $Al_2O_3$  and  $SiO_2$  among the oxides being considered). Some researchers, including Thayne, believe that the InSb bandgap is too narrow (0.17eV), resulting in power dissipation. Unfortunately, high mobility tends to correlate with narrow bandgaps (see Figure 4).

### CV refinement

Thayne believes that solving the gate oxide problem depends on how many people are involved in the research and on improved metrology. There have been a number of cases where the data have been misunderstood by researchers — the metrology suggests that a good device has been produced, but this is not borne out by the transistor's performance.

Last year, the IMEC microelectronics research center in Belgium published research on the widely used CV characterization method, which gives a measure of trap state densities at interfaces [8]. The technique has proven itself for Si-oxide interfaces in CMOS

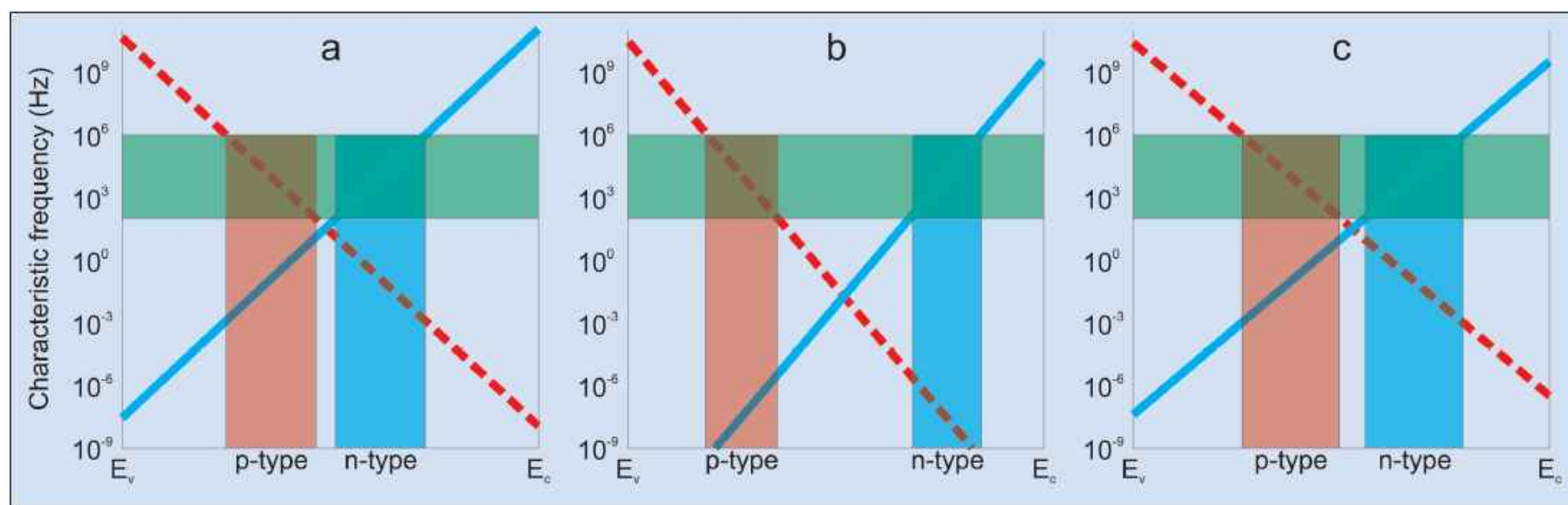


**Figure 4. Bandgap energy at 300K of  $In_xGa_{1-x}As$ , as given by the formula  $(1.42 - 1.49x + 0.43x^2)$ eV [7].**

device characterization over some 30 years. The IMEC paper points out, however, that the method has some fundamental limitations that are not widely known in the research community. This can lead to confusion when the test is applied to GaAs and other III-V MOSFET structures. In particular, there is a strong dependence of the trapping time on the energy depth of the traps within the semiconductor bandgap.

CV measurements are carried out by measuring the capacitance of gate-oxide-semiconductor structures as the voltage is swept repeatedly through a range at various frequencies. Standard equipment covers frequencies from 100Hz to 1MHz. States near the band edge are short lived, but deep levels retain the charge for longer. This gives a characteristic frequency at which the trap will affect the capacitance. The technique gives coverage of the mid-region for Si/ $SiO_2$  structures (Figure 5a), but in GaAs, due to its larger gap, the spread is inadequate (Figure 5b). However, better coverage in GaAs is possible by activating the carriers with a raised temperature (150°C) measurement (Figure 5c). The relatively large gap ensures that large numbers of minority carriers are not generated ( $\sim 10^4 cm^{-3}$ ), avoiding parasitic factors in the measurement. The raised temperature does not significantly increase leakage through the oxide (another possible perturbation).

The IMEC team performed CV measurements on an  $HfO_2/GaAs$  stack at 30°C and 150°C to illustrate these ideas. A 10nm-thick oxide layer was grown on a p-type substrate using atomic layer deposition. The gate material was in the form of 50nm-thick platinum dots deposited through a shadow mask. A layer of AuZn/Au was made on the back side of the substrate to form an ohmic contact. ▶



**Figure 5. Characteristic trapping frequencies for electrons (solid) and holes (dashed) for (a) silicon at 30°C, (b) GaAs at 30°C, and (c) GaAs at 150°C.**

The leakage for both measurements was less than 0.2nA. While the low-temperature measurement naively suggests reasonable interface state densities, the high-temperature data revealed large bumps in depletion at lower frequencies, created by interface states in the mid-region of the gap.

Marc Meuris, one of the leaders of the IMEC work on III-V channels, reports that the team is now investigating ways of passivating oxide layers on both GaAs and InGaAs substrates using a cluster MBE tool. "Although we see improvements in interface states with different treatments, we have not yet found the perfect passivation for III-V materials," he says.

Purdue's Ye believes that CV measurements are still the most effective way to characterize the properties of oxide/III-V interfaces. At higher indium concentrations the bandgap of InGaAs is smaller than that of Si and therefore — all things being equal — CV measurements should have a similar level of effectiveness.

### Aggressive scaling

Having completed its work with Freescale, the Glasgow university is working with a number of industrial partners, such as the companies involved in the Semiconductor Research Corporation (SRC) in the USA and in the European Union's Framework 7 project, involving IBM's Zurich research center, NXP (formerly Philips Semiconductors) and STMicroelectronics. Glasgow is looking to work with others, particularly in Asia. There is some work in Singapore, but the issue is not on the horizon for the big foundries as yet.

Looking at how much time would be needed to validate different gate oxide options and pick the best — and taking the high-k dielectric development for silicon channels that has recently been completed as an analogy — perhaps between three and five years of work are needed.

Glasgow has decided to target the longer-term needs of aggressive device scaling, but also sees possibilities

for spin-offs in areas such as radio frequency power amplification and switch devices. Glasgow has produced GaAs MOSFETs that have similar  $f_T/f_{max}$  performance to pHEMTs but that only need a single power supply. However, further work is needed to supply the wide range of data that is needed on noise, linearity and other factors.

MOSFETs built in other III-V materials may also have applications outside high-performance logic. As an example, professor T Paul Chow of Rensselaer Polytechnic Institute (RPI) is researching gallium nitride MOSFETs using  $\text{SiO}_2$  as the gate oxide for power switching applications. The devices are made using standard tools from a silicon CMOS environment. An NMOS logic inverter has been produced on sapphire substrates using RPI's GaN process, developed by Chow's former PhD student Weixiao Huang. Chow sees such devices being used to implement 'smart power' in power supplies for low-voltage and battery-powered equipment.

The University of Florida has also been doing basic research on improved gate dielectrics for GaN MOSFETs over the past decade or so, under the direction of professor Steve Pearton. Oxides with interface state densities as low as  $1-3 \times 10^{11} \text{cm}^{-2}$  have been produced. Some of the GaN devices have been used to create MOS-HEMT hydrogen detectors. A variety of these HEMTs have been deployed in the field for hydrogen sensing at a Ford dealership in Orlando, where a fleet of hydrogen-fueled cars is stored. ■

### References

- [1] <http://www.itrs.net/>
- [2] Based on formula for  $\text{Ga}_x\text{In}_{1-x}\text{As}$  given at [www.ioffe.rssi.ru/SVA/NSM/Semicond/GaInAs/ebasic.html](http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaInAs/ebasic.html)
- [3] E.g., Hill et al, Electronics Letters, vol.43, p.543, 2007.
- [4] Hill et al, Electronics Letters, vol.44, p.498, 2008.
- [5] Xuan et al, Electron Device Letters, vol.29, p.294, 2008.
- [6] Li et al, App. Phys. Lett., vol.92, p.143507 2008.
- [7] Based on Geotz et al, J. Appl. Phys., vol. 54, p.4543, 1983.
- [8] Brammertz et al. App. Phys. Lett., vol.91, p.133510, 2007.